STM32F405/407/415/417 memories

device	bus	exec	from	to	size	remarks
[remap]	I+D	yes	0x0000 0000	(0x07FF FFFF)		Given by SYSCFG_MEMRMP[1:0]/BOOT pins: 00-FLASH, 01-System FLASH (bootROM), 10-FSMC Bank1 (NOR/PSRAM 1 and 2), 11-SRAM1
FLASH	I+D	yes	0x0800 0000	(0x080F FFFF)	512 kB/1024 kB	Sectors: 4x16kB, 1x64kB, 3x/7x128kB
CCM RAM	D	no	0x1000 0000	0x1000 FFFF	64 kB	not on the bus, accessible only from CPU, needs clock to be enabled in RCC_AHB1ENR.CCMDATARAMEN
System memory (bootROM)	I+D	yes	0x1FFF 0000	0x1FFF 77FF	30 kB	
OTP	I+D	(yes)	0x1FFF 7800	0x1FFF 7A0F	512+16 bytes	16 bytes are locks
Option bytes	I+D	(yes)	0x1FFF C000	0x1FFF C00F	16 bytes	
SRAM1	S	yes	0x2000 0000	0x2001 BFFF	112 kB	[bit-banded onto the 0x22xxxxxx area: bit_addr = 0x22000000 + (byte_addr - 0x20000000) * 32 + (bit_number) * 4]
SRAM2	S	yes	0x2001 C000	0x2001 FFFF	16 kB	[bit-banded onto the 0x22xxxxxx area - see SRAM1]
[bitband area]	S	(no)	0x2200 0000	(0x23FF FFFF)		bit-band area for SRAM1+SRAM2
[peripherals]	S	no	(0x4000 0000)	(0x400F FFFF)		all APB1+APB2 and AHB1 peripherals fit into this area
BKPSRAM	S	no	0x4002 4000	0x4002 4FFF	4 kB	part of the above area; accessed through AHB1 + dedicated regulator must be switched on; battery-backup, tamper-locked, needs clock to be enabled in RCC_AHB1ENR.BKPSRAMEN
[bitband area]	S	no	(0x4200 0000)	(0x43FF FFFF)		bit-band area for the 0x40000000-starting peripherals area (see above)
[peripherals]	S	no	(0x5000 0000)	(0x5FFF FFFF)		AHB2 peripherals (RNG, HASH, CRYP, DCMI)
FSMC NOR/PSRAM1	S	yes	0x6000 0000	(0x63FF FFFF)	up to 64MB	
FSMC NOR/PSRAM2	S	yes	0x6400 0000	(0x67FF FFFF)	up to 64MB	
FSMC NOR/PSRAM3	S	yes	0x6800 0000	(0x6BFF FFFF)	up to 64MB	
FSMC NOR/PSRAM4	S	yes	0x6C00 0000	(0x6FFF FFFF)	up to 64MB	
FSMC NAND BANK2	S	(yes)	0x7000 0000	(0x7FFF FFFF)	up to 64MB	while allocated memory space is 4x64MB, it is split into Common and Attribute spaces
FSMC NAND BANK3	S	(yes)	0x8000 0000	(0x8FFF FFFF)	up to 64MB	while allocated memory space is 4x64MB, it is split into Common and Attribute spaces
FSMC PC CARD	S	(yes)	0x9000 0000	(0x9FFF FFFF)	up to 64MB	while allocated memory space is 4x64MB, it is split into Common and Attribute spaces
FSMC control regs	S	no	0xA000 0000	0xA000 0FFF		
CORE PERIPHERALS	private	no	0xE000 0000	(0xFFFF FFFF)		
there are interesting portions of RAM also in some peripherals:						
ETH FIFO	-	no			2+2 kB	embedded in the ETH peripheral, connected to ETH's DMA, unaccessible directly (only 'F407/417, as 'F405/415 don't have ETH)
OTG_FS FIFO	S	no	0x5002 0000	0x5002 0500	1.25 kB	
OTG_HS FIFO	S	no	0x4006 0000	0x4006 1000	4 kB	
RTC registers	S	no	0x4000 2850	0x4000 289C	80 bytes	battery-backup, tamper-cleared
SDIO FIFO	S	no	0x4001 2C80	0x4001 2CFF	128 bytes	

STM32F405/407/415/417 peripherals

STM32F4xx module	start address	BUS	clock ena	IRQn (vector address = IRQn * 4 + 0x40)				DMA				
Cortex-M4 internal peripherals	0xE0000000	C-M4	no (sysclk)	-1-SysTick	81-FPU							
SYSCFG	0x40013800	APB2	RCC									
PWR	0x40007000	APB1	RCC	1-PVD (EXTI16)								
FSMC control registers	0xA0000000	AHB3	RCC	48-FSMC								
Flash interface registers	0x40023C00	AHB1	RCC	4-FLASH								
DMA1	0x40026000	AHB1	RCC	11-DMA1_Stream0 12-DMA1_Stream1	13-DMA1_Stream2 14-DMA1_Stream3	15-DMA1_Stream4 16-DMA1_Stream5	17-DMA1_Stream6 47-DMA1_Stream7					
DMA2	0x40026400	AHB1	RCC	56-DMA2_Stream0 57-DMA2_Stream1	58-DMA2_Stream2 59-DMA2_Stream3	60-DMA2_Stream4 68-DMA2_Stream5	69-DMA2_Stream6 70-DMA2_Stream7					
DCMI (only 'F4x7)	0x50050000	AHB2	RCC	78-DCMI				DMA2	s1ch1/s7ch1 - DCMI			
USB OTG FS	0x50000000	AHB2	RCC	42-OTG_FS_WKUP (EXTI18)	67-OTG_FS							
USB OTG HS	0x40040000	AHB1	RCC	76-OTG_HS_WKUP (EXTI20)	77-OTG_HS	74-OTG_HS_EP1_OUT	75-OTG_HS_EP1_IN	dedicated DMA				
ETHERNET MAC (only 'F4x7)	0x40028000	AHB1	RCC + external	61-ETH	62-ETH_WKUP (EXTI19)			dedicated DMA				
SDIO	0x40012C00	APB2	RCC	49-SDIO				DMA2	s3ch4/s6ch4 - SDIO			
CAN1	0x40006400	APB1	RCC	19-CAN1_TX	20-CAN1_RX0	21-CAN1_RX1	22-CAN1_SCE					
CAN2	0x40006800	APB1	RCC	63-CAN2_TX	64-CAN2_RX0	65-CAN2_RX1	66-CAN2_SCE					
I2C1	0x40005400	APB1	RCC	31-I2C1_EV	32-I2C1_ER			DMA1	s0ch1/s5ch1 - RX	s6ch1/s7ch1 - TX		
I2C2	0x40005800	APB1	RCC	33-I2C2_EV	34-I2C2_ER			DMA1	s2ch7/s3ch7 - RX	s7ch7 - TX		
I2C3	0x40005C00	APB1	RCC	72-I2C3_EV	73-I2C3_ER			DMA1	s2ch3 - RX	s4ch3 - TX		
SPI1	0x40013000	APB2	RCC	35-SPI1				DMA2	s0ch3/s2ch3 - RX	s3ch3/s5ch3 - TX		
SPI2 / I2S2	0x40003800	APB1	RCC	36-SPI2				DMA1	s3ch0 - RX	s4ch0 - TX		
I2S2ext	0x40003400	APB1	RCC					DMA1	s3ch3 - RX	s4ch2 - TX		
SPI3 / I2S3	0x40003C00	APB1	RCC	51-SPI3				DMA1	s0ch0/s2ch0 - RX	s5ch0/s7ch0 - TX		
I2S3ext	0x40004000	APB1	RCC					DMA1	s0ch3/s2ch2 - RX	s5ch2 - TX		
USART1	0x40011000	APB2	RCC	37-USART1				DMA2	s2ch4/s5ch4 - RX	s7ch4 - TX		
USART2	0x40004400	APB1	RCC	38-USART2				DMA1	s5ch4 - RX	s6ch4 - TX		
USART3	0x40004800	APB1	RCC	39-USART3				DMA1	s1ch4 - RX	s3ch4/s4ch7 - TX		
UART4	0x40004C00	APB1	RCC	52-UART4				DMA1	s2ch4 - RX	s4ch4 - TX		
UART5	0x40005000	APB1	RCC	53-UART5				DMA1	s0ch4 - RX	s7ch4 - TX		
USART6	0x40011400	APB2	RCC	71-USART6				DMA2	s1ch5/s2ch5 - RX	s6ch5/s7ch5 - TX		
TIM1	0x40010000	APB2	RCC	24-TIM1_BRK__TIM9 (shared with TIM9)	25-TIM1_UP__TIM10 (shared with TIM10)	26-TIM1_TRG_COM__TIM11 (shared with TIM11)	27-TIM1_CC	DMA2	s1ch6/s3ch6 - CH1 s2ch6 - CH2 s6ch6 - CH3	s0ch6 - TRIG s5ch6 - UP	s6ch0 - CH1/CH2/CH3	s4ch6 - CH4/TRIG/COM
TIM2	0x40000000	APB1	RCC	28-TIM2				DMA1	s1ch3 - UP/CH3	s5ch3 - CH1	s6ch3 - CH2/CH4	s7ch3 - UP/CH4
TIM3	0x40000400	APB1	RCC	29-TIM3				DMA1	s2ch5 - CH4/UP	s4ch5 - CH1/TRIG	s5ch5 - CH2	s7ch5 - CH3
TIM4	0x40000800	APB1	RCC	30-TIM4				DMA1	s0ch2 - CH1	s3ch2 - CH2	s6ch2 - UP	
TIM5	0x40000C00	APB1	RCC	50-TIM5				DMA1	s0ch6 - CH3/UP s1ch6 - CH4/TRIG	s2ch6 - CH1 s3ch6 - CH4/TRIG	s4ch6 - CH2	s6ch6 - UP
TIM6	0x40001000	APB1	RCC	54-TIM6_DAC				DMA1	s1ch7 - UP			
TIM7	0x40001400	APB1	RCC	55-TIM7				DMA1	s2ch1/s4ch1 - UP			
TIM8	0x40010400	APB2	RCC	43-TIM8_BRK__TIM12 (shared with TIM12)	44-TIM8_UP__TIM13 (shared with TIM13)	45-TIM8_TRG_COM__TIM14 (shared with TIM14)	46-TIM8_CC	DMA2	s1ch7 - UP s2ch7 - CH1	s3ch7 - CH2 s4ch7 - CH3	s2ch0 - CH1/CH2/CH3	s7ch7 - CH4/TRIG/COM
TIM9	0x40014000	APB2	RCC	24-TIM1_BRK__TIM9 (shared with TIM1)								
TIM10	0x40014400	APB2	RCC	25-TIM1_UP__TIM10 (shared with TIM1)								
TIM11	0x40014800	APB2	RCC	26-TIM1_TRG_COM__TIM11 (shared with TIM1)								
TIM12	0x40001800	APB1	RCC	43-TIM8_BRK__TIM12 (shared with TIM8)								
TIM13	0x40001C00	APB1	RCC	44-TIM8_UP__TIM13 (shared with TIM8)								
TIM14	0x40002000	APB1	RCC	45-TIM8_TRG_COM__TIM14 (shared with TIM8)								
RCC	0x40023800	AHB1	no	5-RCC								
RTC & BKP registers	0x40002800	APB1	RCC	2-TAMP_STAMP (EXTI21)	3-RTC_WKUP (EXTI22)		41-RTC_Alarm (EXTI17)					
IWDG	0x40003000	APB1	RCC									
WWDG	0x40002C00	APB1	RCC	0-WWDG								
EXTI	0x40013C00	APB2	no	6-EXTI0 7-EXTI1 8-EXTI2	9-EXTI3 10-EXTI4 23-EXTI9_5	40-EXTI15_10	2-TAMP_STAMP (EXTI21) 3-RTC_WKUP (EXTI22) 41-RTC_Alarm (EXTI17)	1-PVD (EXTI16) 42-OTG_FS_WKUP (EXTI18)			76-OTG_HS_WKUP (EXTI20) 62-ETH_WKUP (EXTI19)	
GPIOA	0x40020000	AHB1	RCC									
GPIOB	0x40020400	AHB1	RCC									
GPIOC	0x40020800	AHB1	RCC									
GPIOD	0x40020C00	AHB1	RCC									
GPIOE	0x40021000	AHB1	RCC									
GPIOF	0x40021400	AHB1	RCC									
GPIOG	0x40021800	AHB1	RCC									
GPIOH	0x40021C00	AHB1	RCC									
GPIOI	0x40022000	AHB1	RCC									
ADC1-ADC2-ADC3	0x40012000	APB2	RCC	18-ADC				DMA2	s0ch0/s4ch0 - ADC1	s2ch1/s3ch1 - ADC2	s0ch2/s1ch2 - ADC3	
DAC	0x40007400	APB1	RCC	54-TIM6_DAC								
CRC	0x40023000	AHB1	RCC									
RNG	0x50060800	AHB2	RCC	80-HASH_RNG								
HASH (only F41x)	0x50060400	AHB2	RCC	80-HASH_RNG				DMA2	s7ch2 - IN			
CRYP (only F41x)	0x50060000	AHB2	RCC	79-CRYP				DMA2	s6ch2 - IN	s5ch2 - OUT		

STM32F405/407/415/417 timers

STM32F4xx	**TIM1**	**TIM2**	**TIM3**	**TIM4**	**TIM5**	**TIM6**	**TIM7**	**TIM8**	**TIM9**	**TIM10**	**TIM11**	**TIM12**	**TIM13**	**TIM14**
type	advanced	gen.purp.32-bit	gen.purp.16-bit	gen.purp.16-bit	gen.purp.32-bit	basic	basic	advanced	2-channel	1-channel	1-channel	2-channel	1-channel	1-channel
counter	16-bit	**32-bit**	16-bit	16-bit	**32-bit**	16-bit	16-bit	16-bit	16-bit	16-bit	16-bit	16-bit	16-bit	16-bit
prescaler	16-bit	16-bit	16-bit	16-bit	16-bit	16-bit	16-bit	16-bit	16-bit	16-bit	16-bit	16-bit	16-bit	16-bit
direction	U, D, U/D	U, D, U/D	U, D, U/D	U, D, U/D	U, D, U/D	U	U	U, D, U/D	U	U	U	U	U	U
base address	0x40010000	0x40000000	0x40000400	0x40000800	0x40000C00	0x40001000	0x40001400	0x40010400	0x40014000	0x40014400	0x40014800	0x40001800	0x40001C00	0x40002000
internal clock source	APB2	APB1	APB1	APB1	APB1	APB1	APB1	APB2	APB2	APB2	APB2	APB1	APB1	APB1
=> max. clk	**168MHz**	84MHz	84MHz	84MHz	84MHz	84MHz	84MHz	**168MHz**	**168MHz**	**168MHz**	**168MHz**	84MHz	84MHz	84MHz
capt./comp. channels	4	4	4	4	4	0	0	4	2	1	1	2	1	1
ETR input	yes	yes	yes	yes	probably no	no	no	yes	no	no	no	no	no	no
slave mode	yes	yes	yes	yes	yes	no	no	yes	yes	no	no	yes	no	no
ITR0	TIM5	TIM1	TIM1	TIM1	TIM2			TIM1	TIM2			TIM4		
ITR1	TIM2	TIM8 (*)	TIM2	TIM2	TIM3			TIM2	TIM3			TIM5		
ITR2	TIM3	TIM3	TIM5	TIM3	TIM4			TIM4	TIM10			TIM13		
ITR3	TIM4	TIM4	TIM4	TIM8	TIM8			TIM5	TIM11			TIM14		
can be master (TRGO to other TIM)?	yes	yes	yes	yes	yes	no	no	yes	no	yes	yes	no	yes	yes
TRGO to DAC?	no	yes	no	yes	yes	yes	yes	yes	no	no	no	no	no	no
TRGO to ADC?	yes (injected)	yes (regul.+inj.)	yes (regular)	yes (injected)	yes (injected)	no	no	yes (regular)	no	no	no	no	no	no
other outputs to ADC?	CC1, CC2, CC3 (regular) + CC4 (injected)	CC2, CC3, CC4 (regular) + CC1 (injected)	CC1 (regular) + CC2, CC4 (injected)	CC4 (regular) + CC1, CC2, CC3 (injected)	CC1, CC2, CC3 (regular) + CC4 (injected)	no	no	CC1 (regular) + CC2, CC3, CC4 (injected)	no	no	no	no	no	no
can trigger DMA?	yes	yes	yes	yes	yes	yes	yes	yes	no	no	no	no	no	no

Remarks:
(*) TIM2_ITR1 can be remapped also to ETH PTP, OTG HS SOF, OTG FS SOF

 V1.6 21 Nov 2019

STM32F405/407/415/417 pins

Pin	LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13		(1)
							SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2ext	SPI3/ I2Sext/I2S3	USART1/2/3/ I2S3ext	UART4/5/USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/OTG_HS	ETH	FSMC/SDIO/ OTG_FS	DCMI	Analog Mode	Notes
PA0	14	C10	23	34	N3	40		TIM2_CH1 TIM2_ETR	TIM5_CH1	TIM8_ETR				USART2_CTS	UART4_TX			ETH_MII_CRS			ADC123_IN0	WKUP (4)(11)
PA1	15	F8	24	35	N2	41		TIM2_CH2	TIM5_CH2					USART2_RTS	UART4_RX			ETH_MII_RX_CLK ETH_RMII_REF_CLK			ADC123_IN1	(4)
PA2	16	J10	25	36	P2	42		TIM2_CH3	TIM5_CH3	TIM9_CH1				USART2_TX				ETH_MDIO			ADC123_IN2	(4)
PA3	17	H9	26	37	R2	47		TIM2_CH4	TIM5_CH4	TIM9_CH2				USART2_RX			OTG_HS_ULPI_D0	ETH_MII_COL			ADC123_IN3	(4)
PA4	20	J9	29	40	N4	50						SPI1_NSS	SPI3_NSS I2S3_WS	USART2_CK					OTG_HS_SOF	DCMI_HSYNC	ADC12_IN4 DAC1_OUT	(3)(4)
PA5	21	G8	30	41	P4	51		TIM2_CH1 TIM2_ETR		TIM8_CH1N		SPI1_SCK					OTG_HS_ULPI_CK				ADC12_IN5 DAC2_OUT	(3)(4)
PA6	22	H8	31	42	P3	52		TIM1_BKIN	TIM3_CH1	TIM8_BKIN		SPI1_MISO				TIM13_CH1				DCMI_PIXCK	ADC12_IN6	(4)
PA7	23	J8	32	43	R3	53		TIM1_CH1N	TIM3_CH2	TIM8_CH1N		SPI1_MOSI				TIM14_CH1		ETH_MII_RX_DV ETH_RMII_CRS_DV			ADC12_IN7	(4)
PA8	41	D1	67	100	F15	119	MCO1	TIM1_CH1			I2C3_SCL			USART1_CK			OTG_FS_SOF					
PA9	42	D2	68	101	E15	120		TIM1_CH2			I2C3_SMBA			USART1_TX						DCMI_D0		OTG_FS_VBUS
PA10	43	D3	69	102	D15	121		TIM1_CH3						USART1_RX			OTG_FS_ID			DCMI_D1		(13)
PA11	44	C1	70	103	C15	122		TIM1_CH4						USART1_CTS		CAN1_RX	OTG_FS_DM					
PA12	45	C2	71	104	B15	123		TIM1_ETR						USART1_RTS		CAN1_TX	OTG_FS_DP					
PA13	46	F8	72	105	A15	124	JTMS-SWDIO															(12) pullup
PA14	49	A2	76	109	A14	137	JTCK-SWCLK															(12) pulldown
PA15	50	B3	77	110	A13	138	JTDI	TIM2_CH1 TIM2_ETR				SPI1_NSS	SPI3_NSS I2S3S_WS									(12) pullup
PB0	26	G7	35	46	R5	56		TIM1_CH2N	TIM3_CH3	TIM8_CH2N							OTG_HS_ULPI_D1	ETH_MII_RXD2			ADC12_IN8	(4)
PB1	27	H7	36	47	R4	57		TIM1_CH3N	TIM3_CH4	TIM8_CH3N							OTG_HS_ULPI_D2	ETH_MII_RXD3			ADC12_IN9	(4)
PB2	28	J7	37	48	M6	58																BOOT1 (9)
PB3	55	B6	89	133	A10	161	JTDO TRACESWO	TIM2_CH2				SPI1_SCK	SPI3_SCK I2S3_CK									(12) floating
PB4	56	A6	90	134	A9	162	NJTRST		TIM3_CH1			SPI1_MISO	SPI3_MISO	I2S3ext_SD								(12) pullup
PB5	57	D7	91	135	A6	163			TIM3_CH2		I2C1_SMBA	SPI1_MOSI	SPI3_MOSI I2S3_SD			CAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT		DCMI_D10		
PB6	58	C7	92	136	B6	164			TIM4_CH1		I2C1_SCL			USART1_TX		CAN2_TX				DCMI_D5		
PB7	59	B7	93	137	B5	165			TIM4_CH2		I2C1_SDA			USART1_RX					FSMC_NL	DCMI_VSYNC		
PB8	61	D8	95	139	A5	167			TIM4_CH3	TIM10_CH1	I2C1_SCL					CAN1_RX		ETH_MII_TXD3	SDIO_D4	DCMI_D6		
PB9	62	C8	96	140	B4	168			TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS I2S2_WS				CAN1_TX			SDIO_D5	DCMI_D7		
PB10	29	H4	47	69	R12	79		TIM2_CH3			I2C2_SCL	SPI2_SCK I2S2_CK		USART3_TX			OTG_HS_ULPI_D3	ETH_MII_RX_ER				
PB11	30	J4	48	70	R13	80		TIM2_CH4			I2C2_SDA			USART3_RX			OTG_HS_ULPI_D4	ETH_MII_TX_EN ETH_RMII_TX_EN				
PB12	33	J3	51	73	P12	92		TIM1_BKIN			I2C2_SMBA	SPI2_NSS I2S2_WS		USART3_CK		CAN2_RX	OTG_HS_ULPI_D5	ETH_MII_TXD0 ETH_RMII_TXD0	OTG_HS_ID			(13)
PB13	34	J1	52	74	P13	93		TIM1_CH1N				SPI2_SCK I2S2_CK		USART3_CTS		CAN2_TX	OTG_HS_ULPI_D6	ETH_MII_TXD1 ETH_RMII_TXD1				OTG_HS_VBUS
PB14	35	J2	53	75	R14	94		TIM1_CH2N		TIM8_CH2N		SPI2_MISO	I2S2ext_SD	USART3_RTS		TIM12_CH1			OTG_HS_DM			
PB15	36	H1	54	76	R15	95	RTC_50Hz	TIM1_CH3N		TIM8_CH3N		SPI2_MOSI I2S2_SD				TIM12_CH2			OTG_HS_DP			
PC0	8	E10	15	26	M2	32											OTG_HS_ULPI_STP				ADC123_IN10	(4)
PC1	9	-	16	27	M3	33												ETH_MDC			ADC123_IN11	(4)
PC2	10	D10	17	28	M4	34						SPI2_MISO	I2S2ext_SD				OTG_HS_ULPI_DIR	ETH_MII_TXD2			ADC123_IN12	(4)
PC3	11	E9	18	29	M5	35						SPI2_MOSI I2S2_SD					OTG_HS_ULPI_NXT	ETH_MII_TX_CLK			ADC123_IN13	(4)
PC4	24	-	33	44	N5	54												ETH_MII_RXD0 ETH_RMII_RXD0			ADC12_IN14	(4)
PC5	25	-	34	45	P5	55												ETH_MII_RXD1 ETH_RMII_RXD1			ADC12_IN15	(4)
PC6	37	F3	63	96	H15	115			TIM3_CH1	TIM8_CH1		I2S2_MCK			USART6_TX				SDIO_D6	DCMI_D0		
PC7	38	E1	64	97	G15	116			TIM3_CH2	TIM8_CH2			I2S3_MCK		USART6_RX				SDIO_D7	DCMI_D1		
PC8	39	E2	65	98	G14	117			TIM3_CH3	TIM8_CH3					USART6_CK				SDIO_D0	DCMI_D2		
PC9	40	E3	66	99	F14	118	MCO2		TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S_CKIN							SDIO_D1	DCMI_D3		
PC10	51	D5	78	111	B14	139							SPI3_SCK I2S3S_CK	USART3_TX	UART4_TX				SDIO_D2	DCMI_D8		
PC11	52	C4	79	112	B13	140						I2S3ext_SD	SPI3_MISO	USART3_RX	UART4_RX				SDIO_D3	DCMI_D4		
PC12	53	A3	80	113	A12	141							SPI3_MOSI I2S3_SD	USART3_CK	UART5_TX				SDIO_CK	DCMI_D9		

Pin	LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13		(1)
							SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2ext	SPI3/ I2Sext/I2S3	USART1/2/3/ I2S3ext	UART4/5/USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/OTG_HS	ETH	FSMC/SDIO/ OTG_FS	DCMI	Analog Mode	Notes
PC13	2	A9	7	7	D1	8																RTC_AF1 (2)(5)(8)
PC14	3	B10	8	8	E1	9																OSC32_IN (2)(5)(6)
PC15	4	B9	9	9	F1	10																OSC32_OUT (2)(5)(6)
PD0	-	D6	81	114	B12	142										CAN1_RX			FSMC_D2			
PD1	-	C5	82	115	C12	143										CAN1_TX			FSMC_D3			
PD2	54	B4	83	116	D12	144			TIM3_ETR						UART5_RX				SDIO_CMD	DCMI_D11		
PD3	-	-	84	117	D11	145								USART2_CTS					FSMC_CLK			
PD4	-	A4	85	118	D10	146								USART2_RTS					FSMC_NOE			
PD5	-	C6	86	119	C11	147								USART2_TX					FSMC_NWE			
PD6	-	B5	87	122	B11	150								USART2_RX					FSMC_NWAIT			
PD7	-	A5	88	123	A11	151								USART2_CK					FSMC_NE1 FSMC_NCE2			
PD8	-	H2	55	77	P15	96								USART3_TX					FSMC_D13			
PD9	-	H3	56	78	P14	97								USART3_RX					FSMC_D14			
PD10	-	G3	57	79	N15	98								USART3_CK					FSMC_D15			
PD11	-	G1	58	80	N14	99								USART3_CTS					FSMC_A16			
PD12	-	G2	59	81	N13	100			TIM4_CH1					USART3_RTS					FSMC_A17			
PD13	-	-	60	82	M15	101			TIM4_CH2										FSMC_A18			
PD14	-	F2	61	85	M14	104			TIM4_CH3										FSMC_D0			
PD15	-	F1	62	86	L14	105			TIM4_CH4										FSMC_D1			
PE0	-	-	97	141	A4	169			TIM4_ETR										FSMC_NBL0	DCMI_D2		
PE1	-	-	98	142	A3	170													FSMC_BLN1	DCMI_D3		
PE2	-	-	1	1	A2	1	TRACECLK											ETH_MII_TXD3	FSMC_A23			
PE3	-	-	2	2	A1	2	TRACED0												FSMC_A19			
PE4	-	-	3	3	B1	3	TRACED1												FSMC_A20	DCMI_D4		
PE5	-	-	4	4	B2	4	TRACED2			TIM9_CH1									FSMC_A21	DCMI_D6		
PE6	-	-	5	5	B3	5	TRACED3			TIM9_CH2									FSMC_A22	DCMI_D7		
PE7	-	G6	38	58	R8	68		TIM1_ETR											FSMC_D4			
PE8	-	H6	39	59	P8	69		TIM1_CH1N											FSMC_D5			
PE9	-	J6	40	60	P9	70		TIM1_CH1											FSMC_D6			
PE10	-	F6	41	63	R9	73		TIM1_CH2N											FSMC_D7			
PE11	-	J5	42	64	P10	74		TIM1_CH2											FSMC_D8			
PE12	-	H5	43	65	R10	75		TIM1_CH3N											FSMC_D9			
PE13	-	G5	44	66	N11	76		TIM1_CH3											FSMC_D10			
PE14	-	F5	45	67	P11	77		TIM1_CH4											FSMC_D11			
PE15	-	G4	46	68	R11	78		TIM1_BKIN											FSMC_D12			
PF0	-	-	-	10	E2	16					I2C2_SDA								FSMC_A0			
PF1	-	-	-	11	H3	17					I2C2_SCL								FSMC_A1			
PF2	-	-	-	12	H2	18					I2C2_SMBA								FSMC_A2			
PF3	-	-	-	13	J2	19													FSMC_A3		ADC3_IN9	(4)
PF4	-	-	-	14	J3	20													FSMC_A4		ADC3_IN14	(4)
PF5	-	-	-	15	K3	21													FSMC_A5		ADC3_IN15	(4)
PF6	-	-	-	18	K2	24				TIM10_CH1									FSMC_NIORD		ADC3_IN4	(4)
PF7	-	-	-	19	K1	25				TIM11_CH1									FSMC_NREG		ADC3_IN5	(4)
PF8	-	-	-	20	L3	26										TIM13_CH1			FSMC_NIOWR		ADC3_IN6	(4)
PF9	-	-	-	21	L2	27										TIM14_CH1			FSMC_CD		ADC3_IN7	(4)
PF10	-	-	-	22	L1	28													FSMC_INTR		ADC3_IN8	(4)
PF11	-	-	-	49	R6	59														DCMI_D12		
PF12	-	-	-	50	P6	60													FSMC_A6			
PF13	-	-	-	53	N6	63													FSMC_A7			
PF14	-	-	-	54	R7	64													FSMC_A8			
PF15	-	-	-	55	P7	65													FSMC_A9			
PG0	-	-	-	56	N7	66													FSMC_A10			
PG1	-	-	-	57	M7	67													FSMC_A11			
PG2	-	-	-	87	L15	106													FSMC_A12			
PG3	-	-	-	88	K15	107													FSMC_A13			
PG4	-	-	-	89	K14	108													FSMC_A14			
PG5	-	-	-	90	K13	109													FSMC_A15			
PG6	-	-	-	91	J15	110													FSMC_INT2			
PG7	-	-	-	92	J14	111									USART6_CK				FSMC_INT3			
PG8	-	-	-	93	H14	112									USART6_RTS			ETH_PPS_OUT				
PG9	-	-	-	124	C10	152									USART6_RX				FSMC_NE2 FSMC_NCE3			
PG10	-	-	-	125	B10	153													FSMC_NCE4_1 FSMC_NE3			
PG11	-	-	-	126	B9	154												ETH_MII_TX_EN ETH_RMII_TX_EN	FSMC_NCE4_2			

Pin	LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13		(1)
							SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2ext	SPI3/ I2Sext/I2S3	USART1/2/3/ I2S3ext	UART4/5/USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/OTG_HS	ETH	FSMC/SDIO/ OTG_FS	DCMI	Analog Mode	Notes
PG12	-	-	-	127	B8	155									USART6_RTS				FSMC_NE4			
PG13	-	-	-	128	A8	156									UART6_CTS			ETH_MII_TXD0 ETH_RMII_TXD0	FSMC_A24			
PG14	-	-	-	129	A7	157									USART6_TX			ETH_MII_TXD1 ETH_RMII_TXD1	FSMC_A25			
PG15	-	-	-	132	B7	160									USART6_CTS					DCMI_D13		
PH0	5	F10	12	23	G1	29																OSC_IN (2)(7)
PH1	6	F9	13	24	H1	30																OSC_OUT (2)(7)
PH2	-	-	-	-	F4	43												ETH_MII_CRS				
PH3	-	-	-	-	G4	44												ETH_MII_COL				
PH4	-	-	-	-	H4	45					I2C2_SCL						OTG_HS_ULPI_NXT					
PH5	-	-	-	-	J4	46					I2C2_SDA											
PH6	-	-	-	-	M11	83					I2C2_SMBA					TIM12_CH1		ETH_MII_RXD2				
PH7	-	-	-	-	N12	84					I2C3_SCL							ETH_MII_RXD3				
PH8	-	-	-	-	M12	85					I2C3_SDA									DCMI_HSYNC		
PH9	-	-	-	-	M13	86					I2C3_SMBA					TIM12_CH2				DCMI_D0		
PH10	-	-	-	-	L13	87			TIM5_CH1											DCMI_D1		
PH11	-	-	-	-	L12	88			TIM5_CH2											DCMI_D2		
PH12	-	-	-	-	K12	89			TIM5_CH3											DCMI_D3		
PH13	-	-	-	-	E12	128				TIM8_CH1N						CAN1_TX						
PH14	-	-	-	-	E13	129				TIM8_CH2N										DCMI_D4		
PH15	-	-	-	-	D13	130				TIM8_CH3N										DCMI_D11		
PI0	-	C3	-	-	E14	131			TIM5_CH4			SPI2_NSS I2S2_WS								DCMI_D13		
PI1	-	B2	-	-	D14	132						SPI2_SCK I2S2_CK								DCMI_D8		
PI2	-	-	-	-	C14	133				TIM8_CH4		SPI2_MISO	I2S2ext_SD							DCMI_D9		
PI3	-	-	-	-	C13	134				TIM8_ETR		SPI2_MOSI I2S2_SD								DCMI_D10		
PI4	-	-	-	-	D4	173				TIM8_BKIN										DCMI_D5		
PI5	-	-	-	-	C4	174				TIM8_CH1										DCMI_VSYNC		
PI6	-	-	-	-	C3	175				TIM8_CH2										DCMI_D6		
PI7	-	-	-	-	C2	176				TIM8_CH3										DCMI_D7		
PI8	-	-	-	-	D2	7																RTC_AF2 (2)(5)(8)
PI9	-	-	-	-	D3	11										CAN1_RX						
PI10	-	-	-	-	E3	12												ETH_MII_RX_ER				
PI11	-	-	-	-	E4	13											OTG_HS_ULPI_DIR					

	60	A7	94	138	D6	166																BOOT0/VPP (9)
	7	G10	14	25	J1	31																NRST (10)
	-	A8	-	143	C6	171																PDR_ON (10)
	-	D9	-	-	L4	-																BYPASS_REG (11)

Notes:

 V1.6 21 Nov 2019

(1) GPIO or Alternate Function or Analog Mode is selected in GPIOx_MODER register for each individual pin. Individual Alternate Function (AF0 to AF15) is selected in GPIOx_AFRL/GPIOx_AFRH registers.
Direction (Output Enable) of a pin when set to Alternate Function is given by the attached peripheral's functionality and is independent of GPIOx_OTYPER register setting.

(2) Alternate Function AF14 is unused. AF15 is EVENTOUT for every pin, except PC13, PC14, PC15, PH0, PH1 and PI8 (oscillator, and battery-backup-domain pins)

(3) Every IO pin is 5V-tolerant, except PA4 and PA5, which are standard 3.3V I/O.
If used as DAC output, PA4 and PA5 should be configured to Analog Mode before enabled (EN1 and EN2 bits in DAC_CR register).

(4) These pins are **not** 5V-tolerant, when in analog mode

(5) PC13, PC14, PC15 and PI8 are part of the battery-backup domain and as such, they are supplied through a power switch. Since the switch only sinks a limited amount of current (3 mA), the use of PC13 to PC15 and PI8 is limited even if used as GPIO output:
- The speed should not exceed 2 MHz with a maximum load of 30 pF.
- These I/Os must not be used as a cu rrent source (e.g. to drive an LED)

(6) PC14, PC15 are **not** 5V-tolerant, when in LSE oscillator mode. Oscillator mode is selected by setting the LSEON bit in the RCC_BDCR register.
GPIO mode for these pins is lost when the 1.2V domain is powered off (by entering standby mode, or removing VDD). In this case these pins are set to analog input mode.

(7) PH0 and PH1 are **not** 5V-tolerant, when in HSE oscillator mode. Oscillator mode is selected by setting the HSEON bit in the RCC_CR register.

(8) PC13 and PI8 pins may have several battery-backup-related alternate functions, which are set in the RTC_CR and RTC_TAFCR registers

(9) State of BOOT[1:0] pins upon reset determines remapping of the lowest address area to boot from FLASH (x0), system memory (boot ROM)(01) or SRAM (11). BOOT0 pin serves as VPP for external programming.

(10) NRST is a bidirectional 5-volt tolerant pin, pulls down for min 20us when internal reset sources are activated (i.e. don't connect to a push-pull external reset circuit). It is permanently connected to a typ. 40kOhm pull-up resistor.
PDR_ON must be high for the internal reset circuitry (including power-up, power-down, brown-out detectors, but also the NRST input!) to be active.

(11) BYPASS_REG if set high, internal regulator is off and 1.2V for core must be supplied externally; in that state PA0 becomes to be an additional reset input and cannot be used as GPIO

(12) PA13, PA14, PA15, PB3, PB4 are after reset in Alternate Mode (to support JTAG right after reset)

(13) PA10 and PB12 have typ. 11kOhm pull-up and pull-down (while all other IO pins have typ. 40kOhm pull-up and pull-down)